A square peg in a round hole: The economics of panel-based lithography for advanced packaging

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Moving from round wafers to rectangular panels saves corner space, delivering a roughly 10% improvement in surface utilization.

We've been doing it for years–square die on round wafers. As the old adage suggests, we can make it work, but it is not always pretty. Now, as advanced packaging processes continue to develop–often adopting and adapting processes and equipment from front-end manufacturing–we need to be sure that we do not needlessly carry over baggage that impedes the optimization of these processes for their new applications. Front-end processes are designed to work on wafers, which are necessarily round and difficult to make larger. In the early days of advanced packaging, these wafer-level processes were extended to the back-end. Fan-in wafer-level chip-scale packaging (WLCSP) and wafer bumping are two prominent examples. However, as advanced packaging processes evolve further into the 2.5D and 3D space, opportunities present themselves to move away from round wafers and onto larger, square or rectangular substrates. Specifically, the manufacturing of fan-out packages on re-constituted substrates populated with KGD (known good die) and the use of high density interposer substrates for so-called 2.5D integration of advanced multi-die packages are experiencing above average growth. For these applications, the substrates can be rectangular and large. In fact, whole industries already exist, such as flat panel displays and solar panels, which

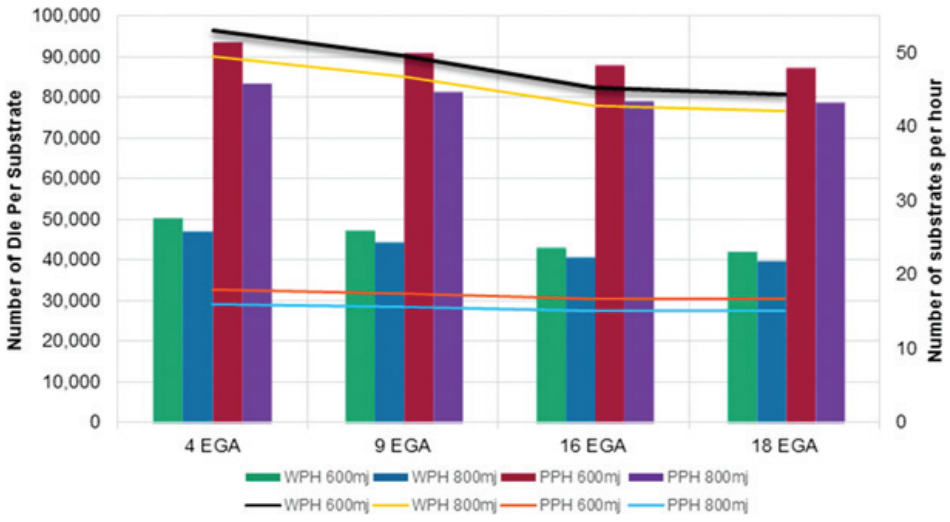

FIGURE 1. Results of throughput comparison.

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use similar manufacturing processes on large rectangular substrates.

In front-end photolithography processes, where square die first met round wafers, there is an inherent inefficiency near the wafer's edge, where squeezing as many die as possible onto the wafer inevitably results in part of the exposure field falling uselessly in the exclusion zone or off the wafer entirely. With an appropriately-sized rectangular substrate the rectangular pattern from the mask could fit perfectly, ultimately increasing the average number of die per exposure and thereby, the throughput of the exposure process. Likewise, using a larger substrate also increases throughput by reducing the nonproductive time spent exchanging substrates. Moreover, the same considerations that have historically driven increases in wafer size should also apply to non-round, non-wafer substrates, potentially providing substantial gains from using large panels throughout the manufacturing process. The flat panel display industry has increased its panel sizes over the years from 400 mm x 500 mm (Gen 2) to 2400mm x 2800mm (Gen 9) and beyond.

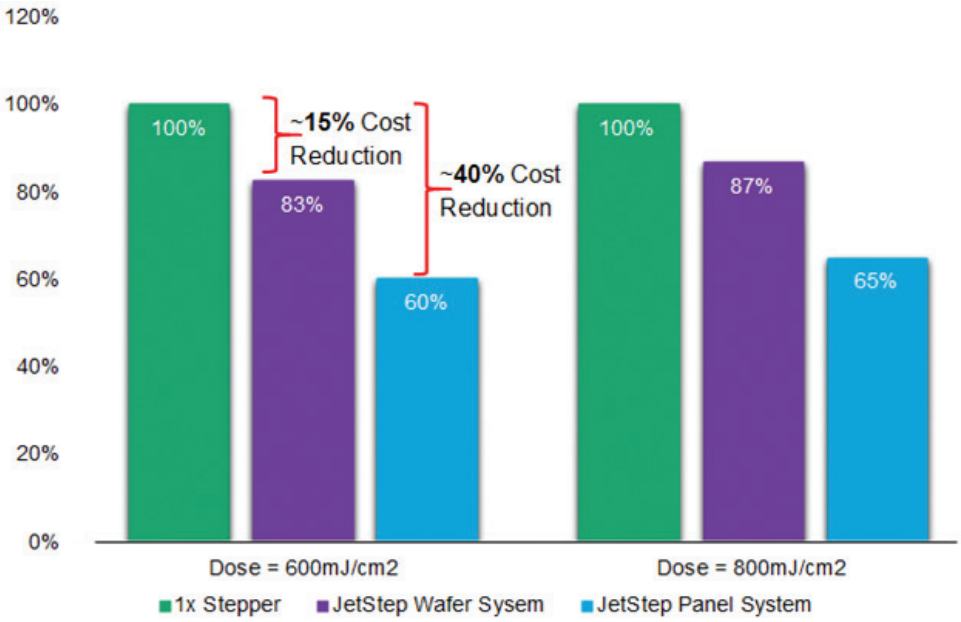

FIGURE 2. Relative cost per 100 die calculated for 8 mm X 8 mm die using 9 alignment points at 600 mj and 800 mj doses.

In an effort to understand the potential economic benefits, we constructed a model to compare the throughput of a 650 mm X 550 mm panel-based lithography process with a 300 mm wafer-based lithography process. The model considered 8 mm square die with 100 µm streets and a 5 mm wafer edge exclusion. We looked at two different mask (reticle) configurations containing 48 die (8 X 6) and 49 die (7 X 7) that could be exposed using the 84 mm diameter field of the 2x reduction JetStep™ Panel Lithography System (Rudolph Technologies). Both mask configurations resulted in 947 die per wafer. Since the square exposure field (7 X 7) required only 23 exposures, 6 less than the 29 exposures required by the rectangular field (8 X 6), all subsequent comparisons use the square field. The panel required 120 exposures resulting in 5214 die. It should be noted that either exposure field configuration was implemented on a standard 6-inch square, .25-inch thick reticle.

The most obvious advantage in the panel process accrues from the more than 5X greater number of substrate exchanges required by the wafer process, resulting primarily from the larger size of the panel substrate. Less obvious, but also important, are two different "square peg in a round hole" effects. The first is the decrease in the number of exposures required that results from the better fit of the rectangular field and the rectangular panel. The second is the increase in surface utilization that results from the better fit between the rectangular die and the rectangular substrate: 947 8 mm die cover 86% of the surface of a 300 mm wafer, whereas 5214 8mm die fill 94% of the surface of a 650 mm X 550 mm panel. A potential disadvantage of the panel process is the requirement for more alignment because of the increased substrate size.

For a more precise comparison, we calculated

	1X Stepper	JetStep Wafer	JetStep Panel
Exposure wavelength	ghi	ghi	ghi
Field size in mm²	68x26	66x52 or 59.4x59.4	66x52 or 59.4x59.4
Substrate size	Wafer 300mm	Wafer 300mm	Panel 650x550mm²
Dose use in mj	600 & 1000	600 & 1000	600 & 1000
Reticle size	6"	6"	6"
Lamp power	2 lamps at 1.2KW	3.5KW	3.5KW
Production parameters	90% uptime and 24/7	90% uptime and 24/7	90% uptime and 24/7
Number of exposures per substrates	44	23	120
Die sizes in mm²	3x3, 8x8, 16x16	3x3, 8x8, 16x16	3x3, 8x8, 16x16

TABLE 1-: Parameters used for FIGURE 2 comparison

throughput in die per hour, assuming each wafer exchange took 15 seconds (including WEP) and each panel exchange took 13 seconds. **FIGURE 1** compares the results for 8 mm X 8 mm die, including evaluation at two different doses (600 mj and 800 mj) and four different numbers of alignment points (4, 9, 16, and 18 points). In all cases, the panel process demonstrated approximately 2X (die per hour) throughput advantage over the wafer process. Predictably, increasing the dosage or the number of alignment points reduced the throughput for both wafer and panel processes. The decrease in throughput associated with increase in number of alignment points had an impact, for example, going from 9 to 16 points at the 600 mj dose reduced throughput by 8.8%.

Next, we estimated the cost-of-ownership for wafer and panel lithography processes, comparing three different wafer exposure systems (1X stepper, Rudolph 2X JetStep System for wafers, and Rudolph 2X JetStep System for panels). **Table 1** shows the parameters used for the comparison. **FIGURE 2** shows the relative cost per 100 die calculated for 8 mm X 8 mm die using 9 alignment points at 600 mj and 800 mj doses. At the 600 mj dose, cost per die decreased by approximately 18% for the JetStep wafer system and nearly 40% for the JetStep panel system, when compared to the 1X stepper. Similarly, at the 800 mj dose, cost per die decreased approximately 13% and 35%. We saw estimated cost savings of similar magnitude for smaller (3 mm X 3 mm) and larger (16 mm X 16 mm) die.

Summary

To summarize, moving from round wafers to rectangular panels ("panel-ization") saves corner space, delivering a roughly 10% improvement in surface utilization. The larger size of the substrate and the improved fit between the mask and substrate reduce the transfer overhead by a factor of 5. The potential reduction in throughput resulting from an increase in the number of alignment points is more than offset by the improvements in throughput. Compared to a 1X stepper on wafers, panel-based processes can reduce lithography cost per die by as much as 40%.

Clearly, there are many aspects of "panel-ization" that must be addressed before these processes gain broad acceptance. It is worth noting that panel lithography is not new. It is widely used in related industries, such as the manufacturing of flat panel displays and photovoltaic solar panels. The JetStep Panel System is built on technology that has over 40 lithography systems currently installed in these and similar applications. As this analysis demonstrates, the potential economic benefits of panel-based lithography are significant. The model discussed here evaluates relatively modest sized panels. Larger panels may offer even greater benefits. Clearly, the transition to panel-based processes for advanced packaging applications bears serious consideration.